SBAS187 – SEPTEMBER 2001

8-Channel, 24-Bit ANALOG-TO-DIGITAL CONVERTER with FLASH Memory

FEATURES

- 24 BITS NO MISSING CODES
- 0.0015% INL
- 22 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- 4K BYTES OF FLASH MEMORY PROGRAMMABLE FROM 2.7V TO 5.25V
- PGA FROM 1 TO 128
- SINGLE CYCLE SETTLING MODE
- PROGRAMMABLE DATA OUTPUT RATES UP TO 1kHz
- PRECISION ON-CHIP 1.25V/2.5V REFERENCE: ACCURACY: 0.2% DRIFT: 5ppm/°C
- EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 2.5V
- ON-CHIP CALIBRATION
- PIN COMPATIBLE WITH ADS1216
- SPI™ COMPATIBLE
- 2.7V TO 5.25V
- < 1mW POWER CONSUMPTION

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION
- WEIGHT SCALES
- PRESSURE TRANSDUCERS

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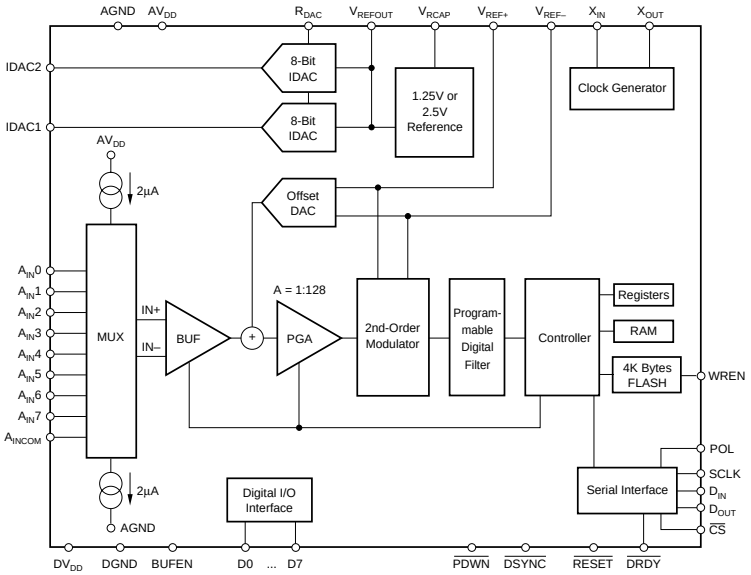
DESCRIPTION

The ADS1218 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution and FLASH memory operating from 2.7V to 5.25V supplies. The delta-sigma, A/D converter provides up to 24 bits of no missing code performance and effective resolution of 22 bits.

The eight input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burn out current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit Digital-to-Analog (D/A) converter provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable sinc filter. The reference input is differential and can be used for ratiometric conversion. The on-board current DACs (Digital-to-Analog Converters) operate independently with the maximum current set by an external resistor.

The serial interface is SPI compatible. Eight bits of digital I/O are also provided that can be used for input or output. The ADS1218 is designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

AV_{DD} to AGND	–0.3V to +6V
DV_{DD} to DGND	–0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
A_{IN}	GND –0.5V to AV_{DD} + 0.5V
AV_{DD} to DV_{DD}	–6V to +6V
AGND to DGND	–0.3V to +0.3V
Digital Input Voltage to GND	–0.3V to DV_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to DV_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Texas Instruments recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1218Y	TQFP-48	PFB	–40°C to +85°C	ADS1218Y	ADS1218Y/250	Tape and Reel, 250
"	"	"	"	"	ADS1218Y/2K	Tape and Reel, 2000

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "ADS1218Y/2K" will get a single 2000-piece Tape and Reel.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications T_{MIN} to T_{MAX}, AV_{DD} = +5V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, f_{OSC} = 2.4576MHz, PGA = 1, Buffer ON, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1218 MIN	ADS1218 TYP	ADS1218 MAX	UNITS
ANALOG INPUT ($A_{IN}0 – A_{IN}7$, A_{INCOM})					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 0.05		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–), See Block Diagram			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		Hz
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		Hz
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		Hz
Programmable Gain Amplifier	User Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		µA
OFFSET DAC					
Offset DAC Range			$\pm V_{REF}/(2 \cdot PGA)$		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±10		%
Offset DAC Gain Error Drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
No Missing Codes	$sinc^3$			24	Bits
Integral Non-Linearity	End Point Fit			±0.0015	% of FS
Offset Error[1]	Before Calibration		7.5		ppm of FS
Offset Drift[1]			0.02		ppm of FS/°C
Gain Error	After Calibration		0.005		%
Gain Error Drift[1]			0.5		ppm/°C
Common-Mode Rejection	at DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Output Noise			See Typical Characteristics		
Power-Supply Rejection	at DC, dB = –20 log($\Delta V_{OUT}/\Delta V_{DD}$)[2]	80	95		dB

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (Cont.)

All specifications T_{MIN} to T_{MAX}, AV_{DD} = +5V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, f_{OSC} = 2.4576MHz, PGA = 1, Buffer ON, R_{DAC} = 150kΩ, f_{DATA} =10Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1218 MIN	ADS1218 TYP	ADS1218 MAX	UNITS
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN–	0		AV_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–)	0.1	2.5	2.6	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	f_{VREFCM} = 60Hz, f_{DATA} = 60Hz		120		dB
Bias Current(3)	V_{REF} = 2.5V		1.3		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	REF HI = 1 at 25°C	2.495	2.50	2.505	V
	REF HI = 0		1.25		V
Short-Circuit Current Source			8		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Noise	BW = 0.1Hz to 100Hz		10		µVp-p
Output Impedance	Sourcing 100µA		3		Ω
Startup Time			50		µs
IDAC					
Full-Scale Output Current	R_{DAC} = 150kΩ, Range = 1		0.5		mA
	R_{DAC} = 150kΩ, Range = 2		1		mA
	R_{DAC} = 150kΩ, Range = 3		2		mA
	R_{DAC} = 15kΩ, Range = 3		20		mA
Maximum Short-Circuit Current Duration	R_{DAC} = 10kΩ		Indefinite		
	R_{DAC} = 0Ω			10	Minutes
Monotonicity	R_{DAC} = 150kΩ	8			Bits
Compliance Voltage		0		AV_{DD} – 1	V
Output Impedance			see Typical Characteristics		
PSRR	V_{OUT} = AV_{DD}/2		400		ppm/V
Absolute Error	Individual IDAC		5		%
Absolute Drift	Individual IDAC		75		ppm/°C
Mismatch Error	Between IDACs, Same Range and Code		0.25		%
Mismatch Drift	Between IDACs, Same Range and Code		15		ppm/°C
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	$\overline{\text{PDWN}}$ = AV_{DD}	4.75		5.25	V
Analog Current (I_{ADC} + I_{VREF} + I_{DAC})	$\overline{\text{PDWN}}$ = 0, or SLEEP		1		nA
ADC Current (I_{ADC})	PGA = 1, Buffer OFF		175	275	µA
	PGA = 128, Buffer OFF		500	750	µA
	PGA = 1, Buffer ON		250	350	µA
	PGA = 128, Buffer ON		900	1375	µA
V_{REF} Current (I_{VREF})			250	375	µA
I_{DAC} Current (I_{DAC})	Excludes Load Current		480	675	µA
Digital Current	Normal Mode, DV_{DD} = 5V		180	275	µA
	SLEEP Mode, DV_{DD} = 5V		150		µA
	Read Data Continuous Mode, DV_{DD} = 5V		230		µA
	$\overline{\text{PDWN}}$= LOW		1		nA
Power Dissipation	PGA = 1, Buffer OFF, REFEN = 0, I_{DACS} OFF, DV_{DD} = 5V		1.8	2.8	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Calibration can minimize these errors. (2) Δ V_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, f_{OSC} = 2.4576MHz, PGA = 1, Buffer ON, R_{DAC} = 75kΩ, f_{DATA}=10Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +1.25V unless otherwise specified.

PARAMETER	CONDITIONS	ADS1218 MIN	ADS1218 TYP	ADS1218 MAX	UNITS
ANALOG INPUT ($A_{IN}0 – A_{IN}7$, A_{INCOM})					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 0.05		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Block Diagram			$\pm V_{REF}$/PGA	V
Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		Hz
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		Hz
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		Hz
Programmable Gain Amplifier	User Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		µA
OFFSET DAC					
Offset DAC Range			$\pm V_{REF}/(2 • PGA)$		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±10		%
Offset DAC Gain Error Drift			2		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
No Missing Codes				24	Bits
Integral Non-Linearity	End Point Fit			±0.0015	% of FS
Offset Error[1]	Before Calibration		15		ppm of FS
Offset Drift[1]			0.04		ppm of FS/°C
Gain Error	After Calibration		0.010		%
Gain Error Drift[1]			1.0		ppm/°C
Common-Mode Rejection	at DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal-Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Output Noise		see Typical Characteristics			
Power-Supply Rejection	at DC, dB = –20 log($\Delta V_{OUT}/\Delta V_{DD}$)[2]	75	90		dB
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN–	0		AV_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–)	0.1		1.25	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	f_{VREFCM} = 60Hz, f_{DATA} = 60Hz		120		dB
Bias Current[3]	V_{REF} = 1.25V		0.65		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	REF HI = 0 at 25°C	1.245	1.25	1.255	V
Short-Circuit Current Source			3		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Noise	BW = 0.1Hz to 100Hz		10		µVp-p
Output Impedance	Sourcing 100µA		3		Ω
Startup Time			50		µs
IDAC					
Full-Scale Output Current	R_{DAC} = 75kΩ, Range = 1		0.5		mA
	R_{DAC} = 75kΩ, Range = 2		1		mA
	R_{DAC} = 75kΩ, Range = 3		2		mA
	R_{DAC} = 15kΩ, Range = 3		20		mA
Maximum Short-Circuit Current Duration	R_{DAC} = 10kΩ		Indefinite		
	R_{DAC} = 0Ω			10	Minute
Monotonicity	R_{DAC} = 75kΩ	8			Bits
Compliance Voltage		0		AV_{DD} – 1	V
Output Impedance		see Typical Characteristics			
PSRR	V_{OUT} = AV_{DD}/2		600		ppm/V
Absolute Error	Individual IDAC		5		%
Absolute Drift	Individual IDAC		75		ppm/°C
Mismatch Error	Between IDACs, Same Range and Code		0.25		%
Mismatch Drift	Between IDACs, Same Range and Code		15		ppm/°C

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V (Cont.)

All specifications T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, f_{OSC} = 2.4576MHz, PGA = 1, Buffer ON, R_{DAC} = 75kΩ, f_{DATA}=10Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +1.25V unless otherwise specified.

PARAMETER	CONDITIONS	ADS1218 MIN	ADS1218 TYP	ADS1218 MAX	UNITS
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	2.7		3.3	V
Analog Current (I_{ADC} + I_{VREF} + I_{DAC})	$\overline{PDWN}$ = 0, or SLEEP		1		nA
ADC Current (I_{ADC})	PGA = 1, Buffer OFF		160	250	µA
	PGA = 128, Buffer OFF		450	700	µA
	PGA = 1, Buffer ON		230	325	µA
	PGA = 128, Buffer ON		850	1325	µA
V_{REF} Current (I_{VREF})			250	375	µA
I_{DAC} Current (I_{DAC})	Excludes Load Current		480	675	µA
Digital Current	Normal Mode, DV_{DD} = 3V		90	200	µA
	SLEEP Mode, DV_{DD} = 3V		75		µA
	Read Data Continuous Mode, DV_{DD} = 3V		113		µA
	$\overline{PDWN}$ = 0		1		nA
Power Dissipation	PGA = 1, Buffer OFF, REFEN = 0, I_{DACS} OFF, DV_{DD} = 3V		0.8	1.4	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Calibration can minimize these errors. (2) Δ V_{OUT} is change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

DIGITAL CHARACTERISTICS: T_{MIN} to T_{MAX}, DV_{DD} = 2.7V to 5.25V

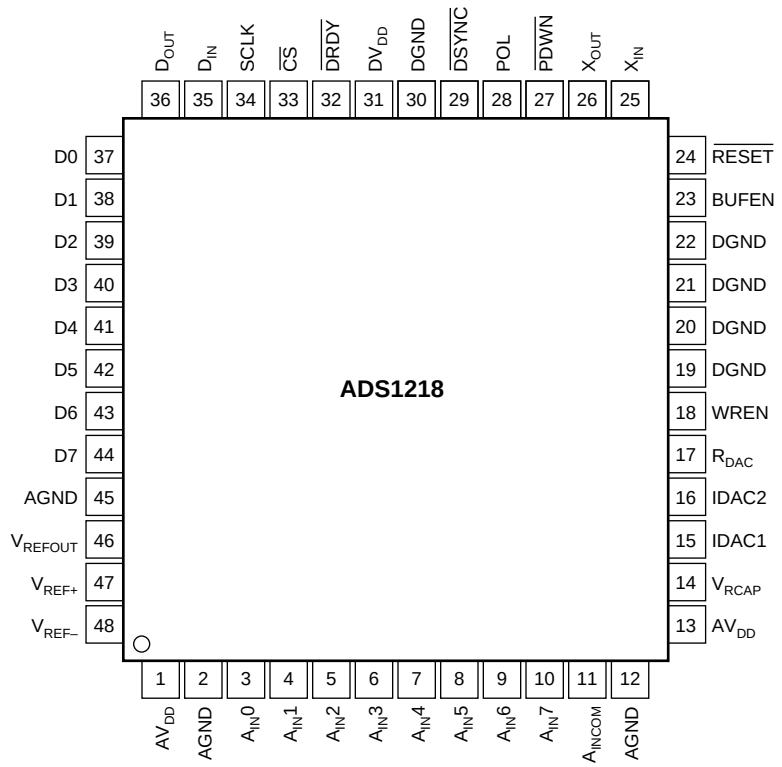
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input/Output					
Logic Family			CMOS		
Logic Level: V_{IH}		0.8 • DV_{DD}		DV_{DD}	V
V_{IL}		DGND		0.2 • DV_{DD}	V
V_{OH}	I_{OH} = 1mA	DV_{DD} – 0.4			V
V_{OL}	I_{OL} = 1mA	DGND		DGND + 0.4	V
Input Leakage: I_{IH}	V_I = DV_{DD}			10	µA
I_{IL}	V_I = 0	–10			µA
Master Clock Rate: f_{OSC}(1)		1		5	MHz
Master Clock Period: t_{OSC}(1)	$1/f_{OSC}$	200		1000	ns

NOTE: (1) For FLASH E/W operations, the SPEED bit in the SETUP register must be set appropriately and the device operating frequency must be: 2.3MHz < F_{OSC} < 4.13MHz.

FLASH CHARACTERISTICS: T_{MIN} to T_{MAX}, DV_{DD} = 2.7V to 5.25V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current					
Page Write	DV_{DD} = 5V, During WR2F Command		6.5		mA
	DV_{DD} = 3V, During WR2F Command		3.75		mA
Page Read	DV_{DD} = 5V, During RF2R Command		4.0		mA
	DV_{DD} = 3V, During RF2R Command		1.2		mA
Endurance			100,000		E/W Cycles
Data Retention	at 25°C	100			Years
DV_{DD} for Erase/Write		2.7		5.25	V

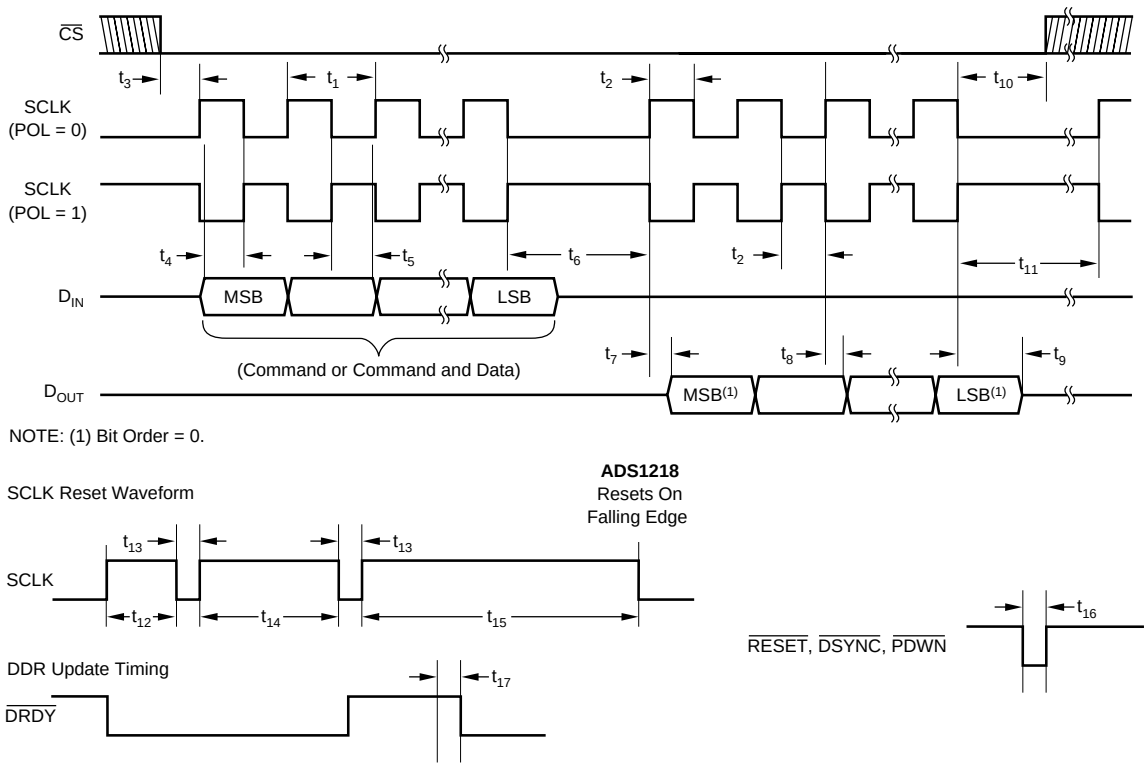
PIN CONFIGURATION (TQFP-48)



PIN DESCRIPTIONS

PIN NUMBER	NAME	DESCRIPTION	PIN NUMBER	NAME	DESCRIPTION
1	AV_{DD}	Analog Power Supply	24	$\overline{RESET}$	Active LOW, resets the entire chip.
2	AGND	Analog Ground	25	X_{IN}	Clock Input
3	$A_{IN}0$	Analog Input 0	26	X_{OUT}	Clock Output, used with crystal or resonator.
4	$A_{IN}1$	Analog Input 1	27	$\overline{PDWN}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
5	$A_{IN}2$	Analog Input 2			
6	$A_{IN}3$	Analog Input 3			
7	$A_{IN}4$	Analog Input 4	28	POL	Serial Clock Polarity
8	$A_{IN}5$	Analog Input 5	29	$\overline{DSYNC}$	Active LOW, Synchronization Control
9	$A_{IN}6$	Analog Input 6	30	DGND	Digital Ground
10	$A_{IN}7$	Analog Input 7	31	DV_{DD}	Digital Power Supply
11	A_{INCOM}	Analog Input Common	32	$\overline{DRDY}$	Active LOW, Data Ready
12	AGND	Analog Ground	33	$\overline{CS}$	Active LOW, Chip Select
13	AV_{DD}	Analog Power Supply	34	SCLK	Serial Clock, Schmitt Trigger
14	V_{RCAP}	V_{REF} Bypass CAP	35	D_{IN}	Serial Data Input, Schmitt Trigger
15	IDAC1	Current DAC1 Output	36	D_{OUT}	Serial Data Output
16	IDAC2	Current DAC2 Output	37-44	D0-D7	Digital I/O 0-7
17	R_{DAC}	Current DAC Resistor	45	AGND	Analog Ground
18	WREN	Active High, FLASH Write Enable	46	V_{REFOUT}	Voltage Reference Output
19-22	DGND	Digital Ground	47	V_{REF+}	Positive Differential Reference Input
23	BUFEN	Buffer Enable	48	$V_{REF–}$	Negative Differential Reference Input

TIMING SPECIFICATIONS



TIMING SPECIFICATION TABLES

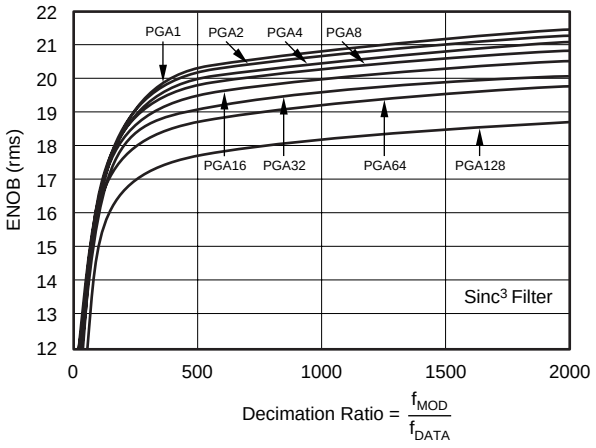
SPEC	DESCRIPTION	MIN	MAX	UNITS
t_1	SCLK Period	4		t_{OSC} Periods
			3	$\overline{DRDY}$ Periods
t_2	SCLK Pulse Width, HIGH and LOW	200		ns
t_3	$\overline{CS}$ LOW to first SCLK Edge; Setup Time	0		ns
t_4	D_{IN} Valid to SCLK Edge; Setup Time	50		ns
t_5	Valid D_{IN} to SCLK Edge; Hold Time	50		ns
t_6	Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT}:			
	RDATA, RDATAC, RREG, WREG, RRAM, WRAM	50		t_{OSC} Periods
	CSREG, CSRAMX, CSRAM	200		t_{OSC} Periods
	CHKARAM, CHKARAMX	1100		t_{OSC} Periods
t_7(1)	SCLK Edge to Valid New D_{OUT}		50	ns
t_8(1)	SCLK Edge to D_{OUT}, Hold Time	0		ns
t_9	Last SCLK Edge to D_{OUT} Tri-State	6	10	t_{OSC} Periods
	NOTE: D_{OUT} goes tri-state immediately when $\overline{CS}$ goes HIGH.			
t_{10}	$\overline{CS}$ LOW time after final SCLK edge	0		ns
t_{11}	Final SCLK edge of one op code until first edge SCLK of next command:			
	RREG, WREG, RRAM, WRAM, CSRAMX, CSARAMX, CSRAM, CSARAM, CSREG, SLEEP, RDATA, RDATAC, STOPC	4		t_{OSC} Periods
	DSYNC, RESET	16		t_{OSC} Periods
	CSFL	33,000		t_{OSC} Periods
	CREG, CRAM	220		t_{OSC} Periods
	RF2R	1090		t_{OSC} Periods
	CREGA	1600		t_{OSC} Periods
	WR2F	76,850 (SPEED = 0)		t_{OSC} Periods
		101,050 (SPEED = 1)	4	t_{OSC} Periods
	SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL	7		$\overline{DRDY}$ Periods
	SELFCAL	14		$\overline{DRDY}$ Periods
	RESET (Command, SCLK, or Pin)	16		t_{OSC} Periods
t_{12}	SCLK Reset, First HIGH Pulse	300	500	t_{OSC} Periods
t_{13}	SCLK Reset, LOW Pulse	5		t_{OSC} Periods
t_{14}	SCLK Reset, Second HIGH Pulse	550	750	t_{OSC} Periods
t_{15}	SCLK Reset, Third HIGH Pulse	1050	1250	t_{OSC} Periods
t_{16}	Pulse Width	4		t_{OSC} Periods
t_{17}	DOR Data Not Valid	4		t_{OSC} Periods

NOTE: (1) Load = 20pF ||10kΩ to DGND.

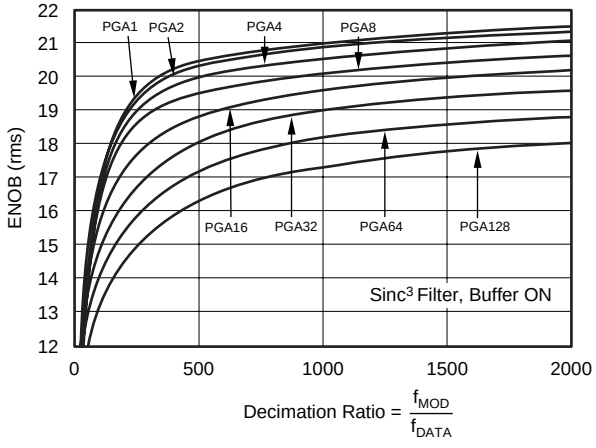
TYPICAL CHARACTERISTICS

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

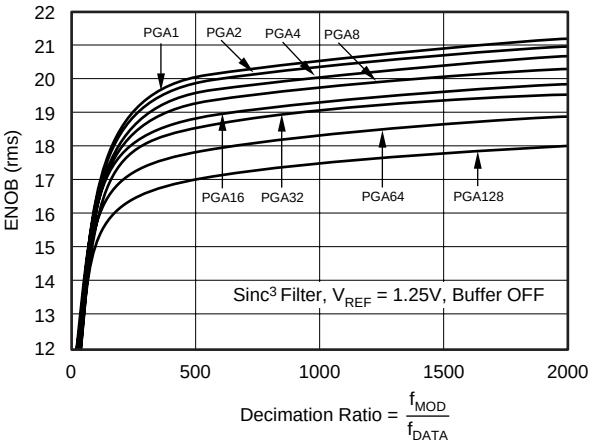
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



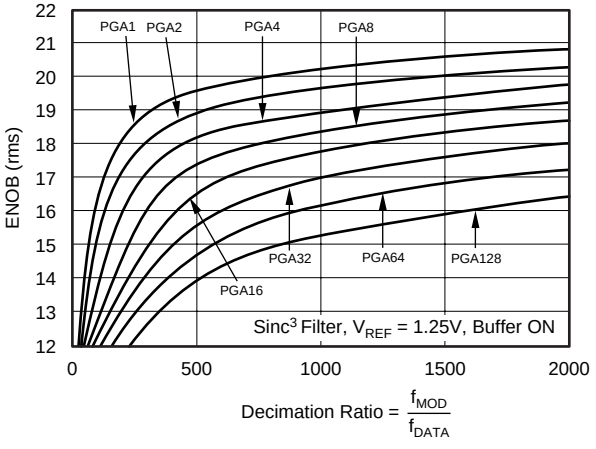
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



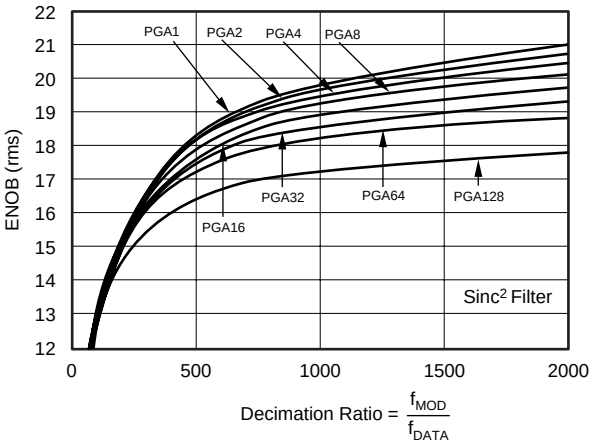
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



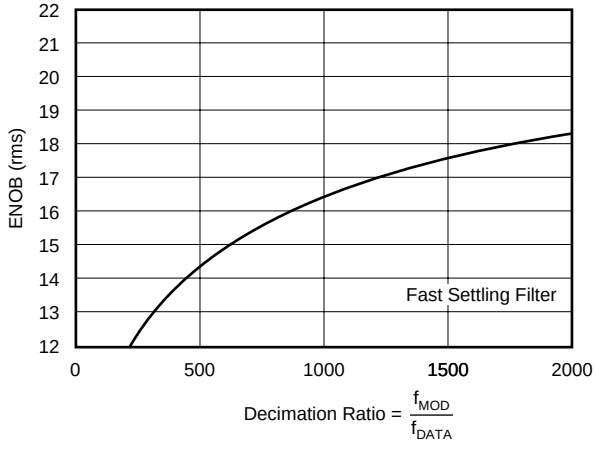
EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



EFFECTIVE NUMBER OF BITS
vs DECIMATION RATIO



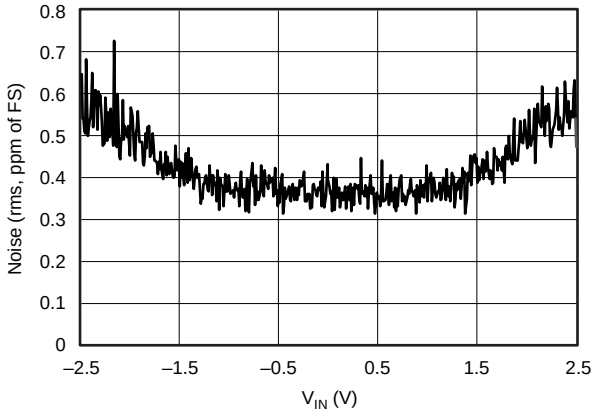
FAST SETTLING FILTER
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



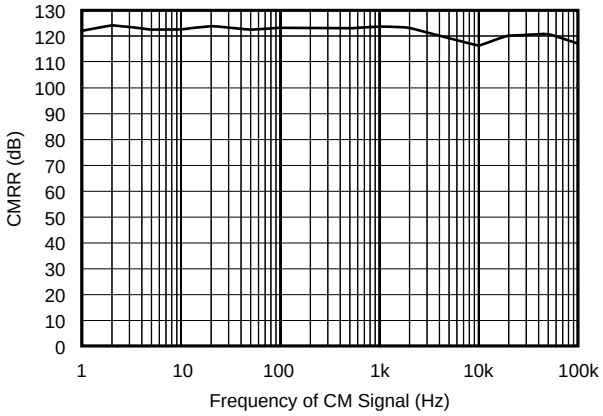
TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

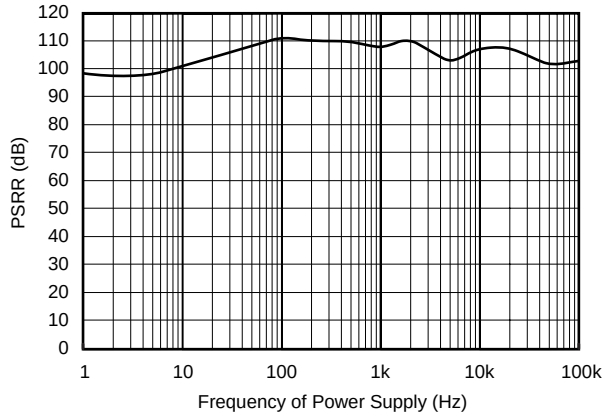
NOISE vs INPUT SIGNAL



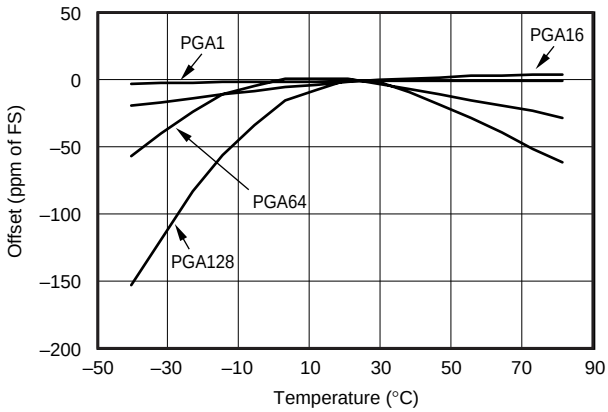
CMRR vs FREQUENCY



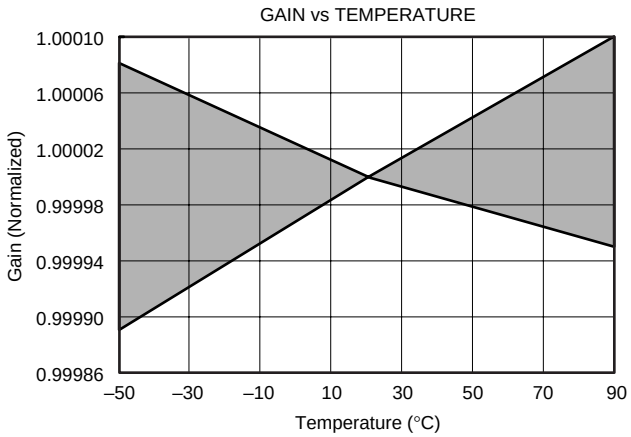
PSRR vs FREQUENCY



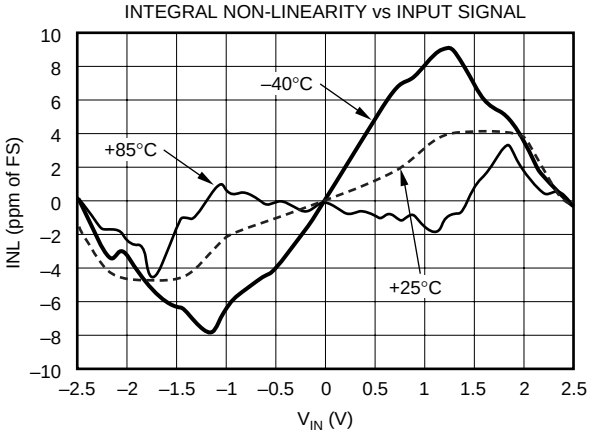
OFFSET vs TEMPERATURE



GAIN vs TEMPERATURE



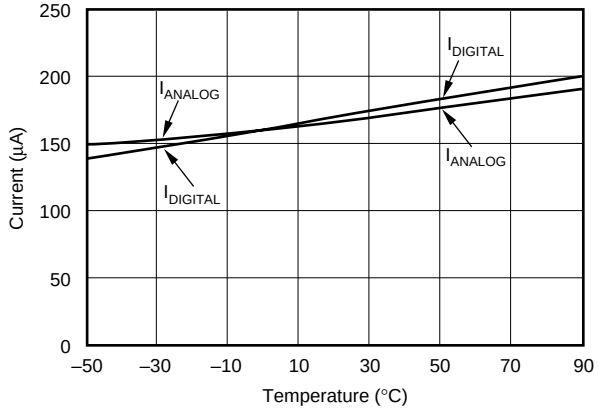
INTEGRAL NON-LINEARITY vs INPUT SIGNAL



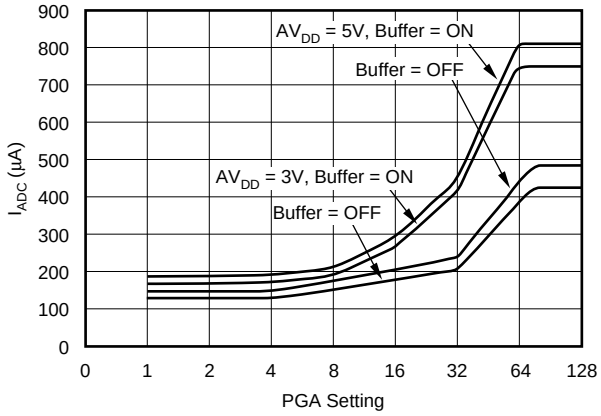
TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

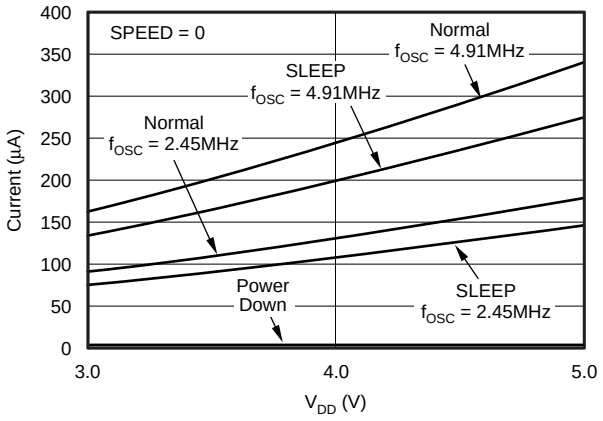
CURRENT vs TEMPERATURE



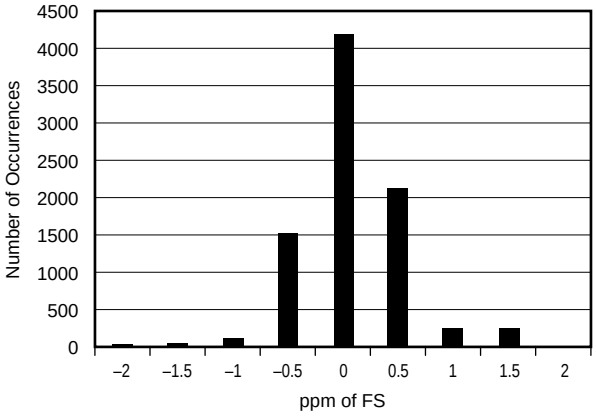
ADC CURRENT vs PGA



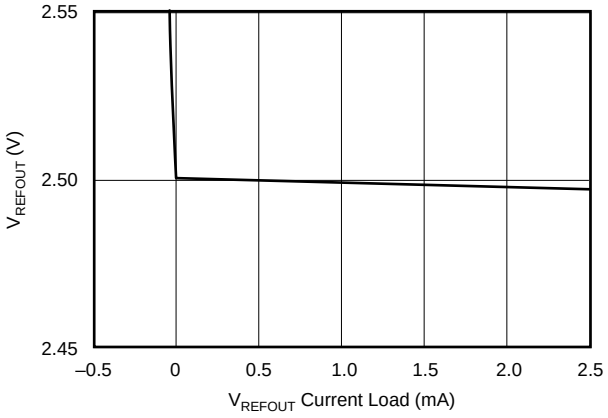
DIGITAL CURRENT



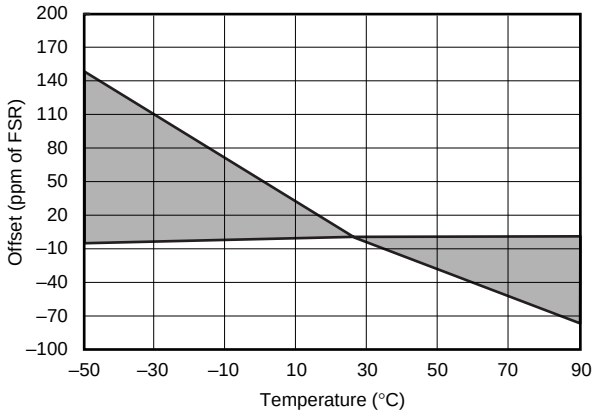
HISTOGRAM OF OUTPUT DATA



V_{REFOUT} vs LOAD CURRENT



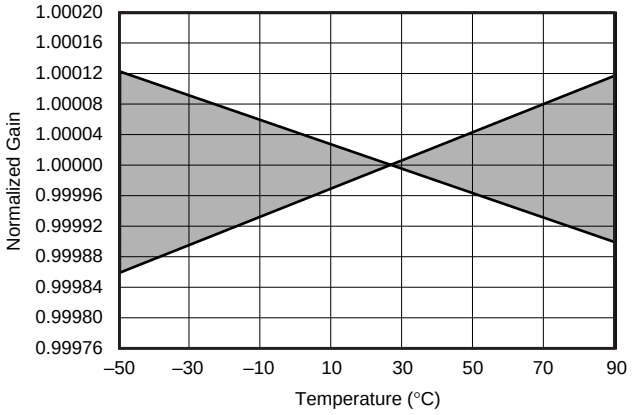
OFFSET DAC - OFFSET vs TEMPERATURE



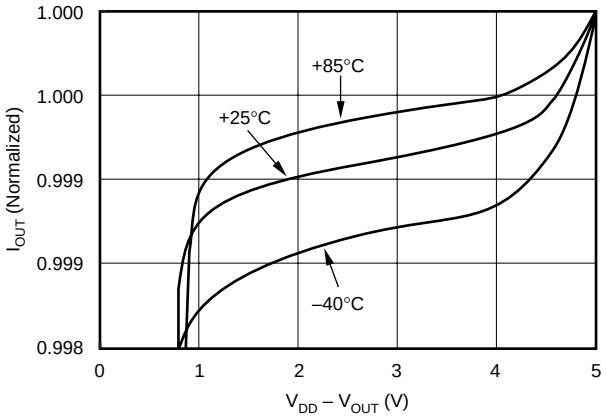
TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, R_{DAC} = 150kΩ, f_{DATA} = 10Hz, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

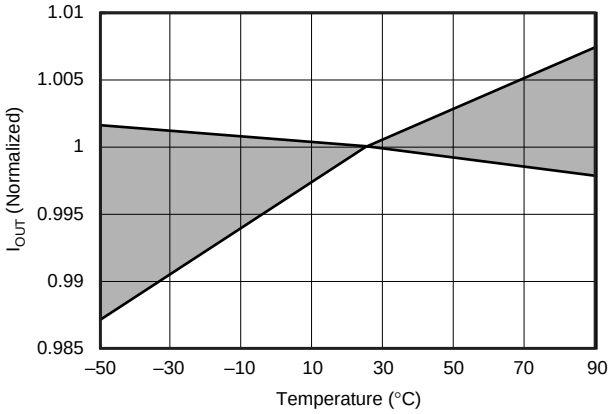
OFFSET DAC - GAIN vs TEMPERATURE



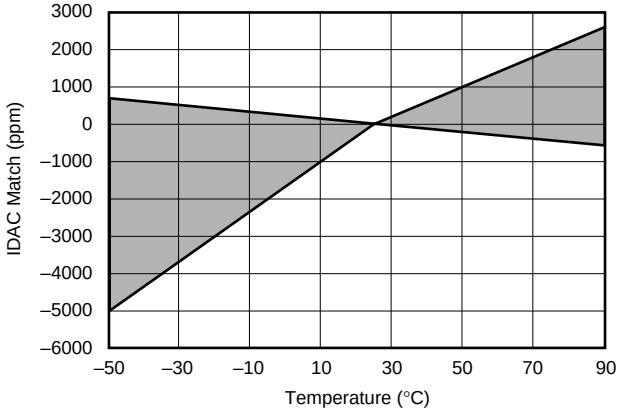
IDAC R_{OUT} vs V_{OUT}



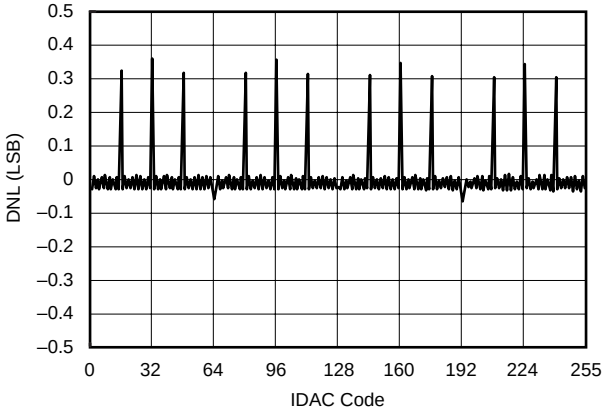
IDAC NORMALIZED vs TEMPERATURE



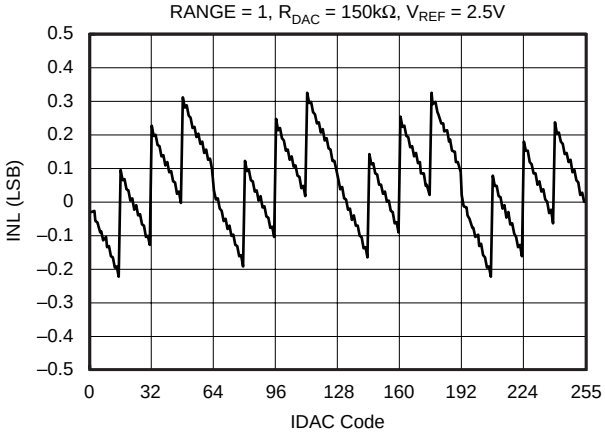
IDAC MATCHING vs TEMPERATURE



IDAC DIFFERENTIAL NON-LINEARITY
RANGE = 1, R_{DAC} = 150kΩ, V_{REF} = 2.5V



IDAC INTEGRAL NON-LINEARITY
RANGE = 1, R_{DAC} = 150kΩ, V_{REF} = 2.5V



OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. For example, if channel 1 is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to eight fully differential input channels.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the input pins.

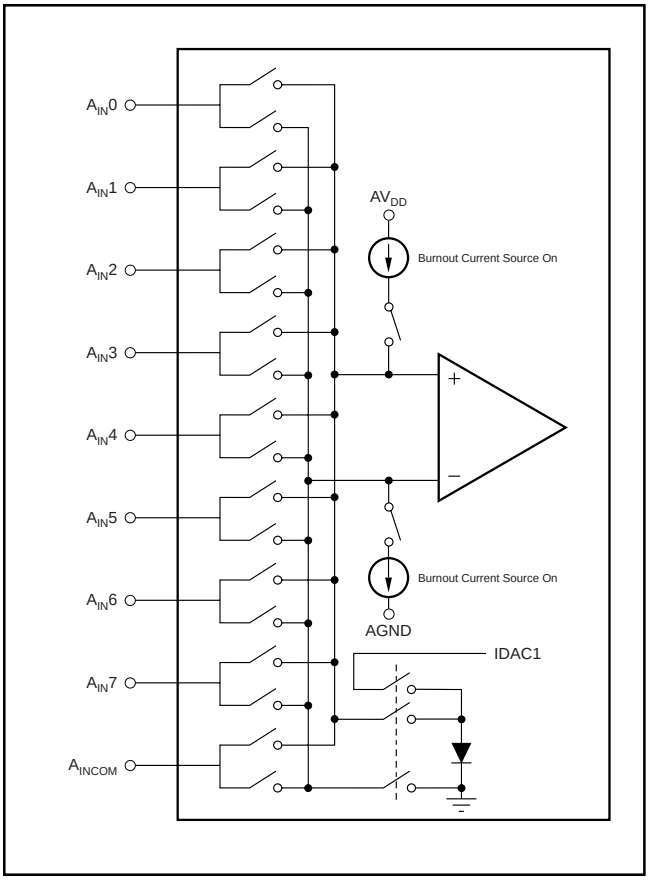


FIGURE 1. Input Multiplexer Configuration.

TEMPERATURE SENSOR

An on-chip diode provides temperature sensing capability. When the configuration register for the input MUX is set to all 1s, the diode is connected to the input of the A/D converter. All other channels are open. The anode of the diode is connected to the positive input of the A/D converter, and the cathode of the diode is connected to negative input of the A/D converter. The output of IDAC1 is connected to the anode to bias the diode and the cathode of the diode is also connected to ground to complete the circuit.

In this mode, the output of IDAC1 is also connected to the output pin, so some current may flow into an external load from IDAC1, rather than the diode.

BURNOUT CURRENT SOURCES

When the Burnout bit is set in the ACR configuration register, two current sources are enabled. The current source on the positive input channel sources approximately 2µA of current. The current source on the negative input channel sinks approximately 2µA. This allows for the detection of an open circuit (full-scale reading) or short circuit (0V differential reading) on the selected input differential pair.

INPUT BUFFER

The input impedance of the ADS1218 without the buffer is 5MΩ/PGA. With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. The buffer is controlled by ANDing the state of the BUFEN pin with the state of the BUFFER bit in the ACR register.

IDAC1 AND IDAC2

The ADS1218 has two 8-bit current output DACs that can be controlled independently. The output current is set with R_{DAC}, the range select bits in the ACR register, and the 8-bit digital value in the IDAC register. The output current = $V_{REF}/(8 \bullet R_{DAC})(2^{RANGE-1})$(DAC CODE). With V_{REFOUT} = 2.5V and R_{DAC} = 150kΩ to AGND the full-scale output can be selected to be 0.5, 1, or 2mA. The compliance voltage range is 0 to within 1V of AV_{DD}. When the internal voltage reference of the ADS1218 is used, it is the reference for the IDAC. An external reference may be used for the IDACs by disabling the internal reference and tying the external reference input to the V_{REFOUT} pin.

PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale range, the A/D converter can resolve to 1µV. With a PGA of 128, on a 40mV full-scale range, the A/D converter can resolve to 75nV. With a PGA of 1 on a 5V full-scale range, it would require a 26-bit A/D converter to resolve 75nV.

PGA OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA by using the ODAC register. The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the ODAC register does not reduce the performance of the A/D converter.

MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the SETUP register.

SPEED BIT	f_{MOD}
0	$f_{OSC}/128$
1	$f_{OSC}/256$

CALIBRATION

The offset and gain errors in the ADS1218, or the complete system, can be reduced with calibration. Internal calibration of the ADS1218 is called self calibration. This is handled with three commands. One command does both offset and gain calibration. There is also a gain calibration command and an offset calibration command. Each calibration process takes seven t_{DATA} periods to complete. Therefore, it takes 14 t_{DATA} periods to complete both an offset and gain calibration.

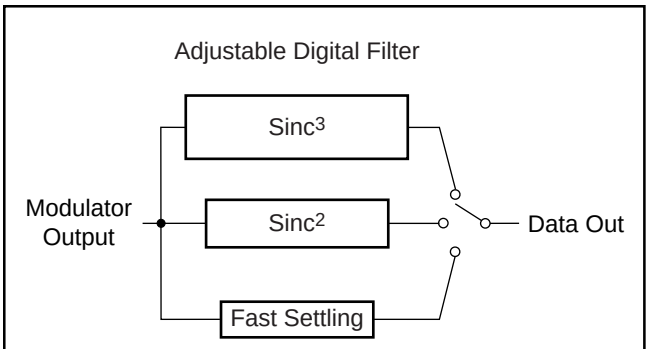
For system calibration, the appropriate signal must be applied to the inputs. The system offset command requires a "zero" differential input signal. It then computes an offset that will nullify offset in the system. The system gain command requires a positive "full-scale" differential input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

Calibration should be performed after power on, a change in temperature, a change in decimation ratio, or a change in the PGA. Calibration will remove the offset in the ODAC register. Therefore, changes to the ODAC register must be done after calibration.

At the completion of calibration, the DRDY signal will go LOW to indicate that calibration is complete and valid data is available.

DIGITAL FILTER

The Digital Filter can use either the fast settling, sinc^2, or sinc^3 filter, as shown in Figure 2. In addition, the Auto mode changes the sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the fast settling filter for the next two conversions, the first of which should be discarded. It will then use the sinc^2 followed by the sinc^3 filter to improve noise performance. This combines the low-noise advantage of the sinc^3 filter with the quick response of the fast settling time filter. The frequency response of each filter is shown in Figure 3.



FILTER SETTLING TIME

FILTER	SETTLING TIME (Conversion Cycles)
Sinc^3	3(1)
Sinc^2	2(1)
Fast	1(1)

NOTE: (1) With Synchronized Channel Changes.

AUTO MODE FILTER SELECTION

CONVERSION CYCLE			
1	2	3	4+
Discard	Fast	Sinc^2	Sinc^3

FIGURE 2. Filter Step Responses.

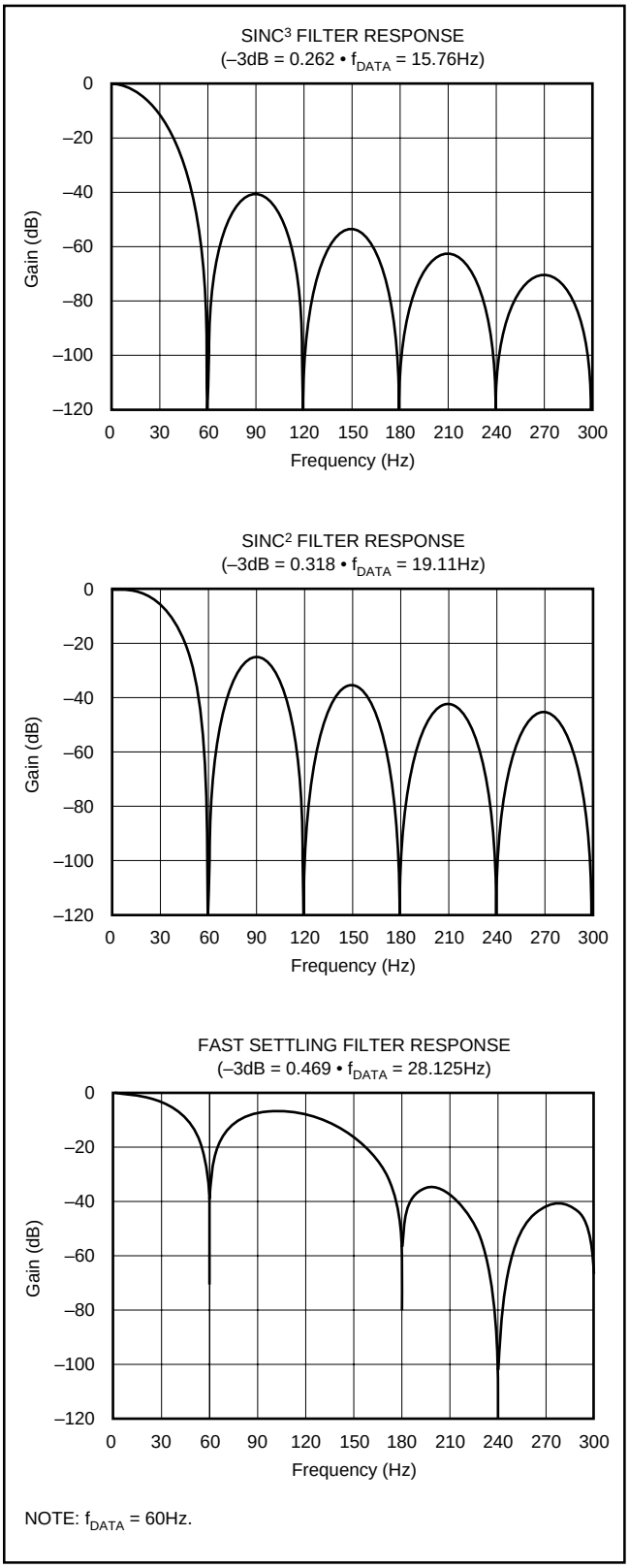


FIGURE 3. Filter Frequency Responses.

VOLTAGE REFERENCE

The voltage reference used for the ADS1218 can either be internal or external. The power-up configuration for the voltage reference is 2.5V internal. The selection for the voltage reference is made through the status configuration register.

The internal voltage reference is selectable as either 1.25V or 2.5V (AV_{DD} = 5V only). The V_{REFOUT} pin should have a 0.1µF capacitor to AGND.

The external voltage reference is differential and is represented by the voltage difference between the pins: $+V_{REF}$ and $-V_{REF}$. The absolute voltage on either pin ($+V_{REF}$ and $-V_{REF}$) can range from AGND to AV_{DD}, however, the differential voltage must not exceed 2.5V. The differential voltage reference provides easy means of performing ratiometric measurement.

V_{RCAP} PIN

This pin provides a bypass cap for noise filtering on internal V_{REF} circuitry only. The recommended capacitor is a 0.001µF ceramic cap. If an external V_{REF} is used, this pin can be left unconnected.

CLOCK GENERATOR

The clock source for the ADS1218 can be provided from a crystal, ceramic resonator, oscillator, or external clock. When the clock source is a crystal or ceramic resonator, external capacitors must be provided to ensure start-up and a stable clock frequency. This is shown in Figure 4 and Table I.

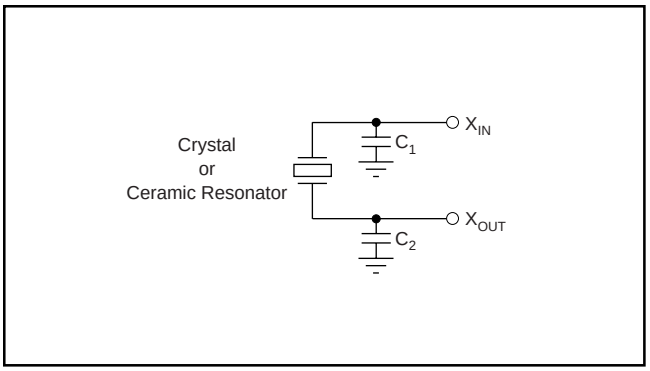


FIGURE 4. Crystal or Ceramic Resonator Connection.

CLOCK SOURCE	FREQUENCY	C_1	C_2	PART NUMBER
Crystal	2.4576	0-20pF	0-20pF	ECS, ECSD 2.45 - 32
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSL 4.91
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSD 4.91
Crystal	4.9152	0-20pF	0-20pF	CTS, MP 042 4M9182

TABLE I. Typical Clock Sources.

DIGITAL I/O INTERFACE

The ADS1218 has eight pins dedicated for digital I/O. The default power-up condition for the digital I/O pins are as inputs. All of the digital I/O pins are individually configurable as inputs or outputs. They are configured through the DIR control register. The DIR register defines whether the pin is an input or output, and the DIO register defines the state of the digital output. When the digital I/O are configured as inputs, DIO is used to read the state of the pin.

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (D_{IN}, D_{OUT}, SCLK, and $\overline{CS}$). The ADS1218 also offers the flexibility to select the polarity of the serial clock through the POL pin. The serial interface can be clocked up to $f_{OSC}/4$. If $\overline{CS}$ goes HIGH, the serial interface is reset. When $\overline{CS}$ goes LOW, a new command is expected.

The serial interface operates independently of $\overline{DRDY}$. $\overline{DRDY}$ is used to indicate availability of data in the DOR. In order to ensure the validity of the data being read, DOR timing requirements must be met.

$\overline{DSYNC}$ OPERATION

$\overline{DSYNC}$ is used to provide for synchronization of the A/D conversion with an external event. Synchronization can be achieved either through the $\overline{DSYNC}$ pin or the $\overline{DSYNC}$ command. When the $\overline{DSYNC}$ pin is used, the filter counter is reset on the falling edge of $\overline{DSYNC}$. The modulator is held in reset until $\overline{DSYNC}$ is taken HIGH. Synchronization occurs on the next rising edge of the system clock after $\overline{DSYNC}$ is taken HIGH.

When the $\overline{DSYNC}$ command is sent, the filter counter is reset after the last SCLK on the $\overline{DSYNC}$ command. The modulator is held in RESET until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK after the $\overline{DSYNC}$ command.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically. The POR issues the RESET command as described below.

$\overline{RESET}$

There are three methods of reset. The $\overline{RESET}$ pin, the RESET command, and the SCLK Reset pattern. They all perform the same function. After a reset, the FLASH data values from Page 0 are loaded into RAM, subsequently data values from Bank 0 of RAM are loaded into the configuration registers.

MEMORY

Three types of memory are used on the ADS1218: registers, RAM, and FLASH. 16 registers directly control the various functions (PGA, DAC value, Decimation Ratio, etc.) and can be directly read or written to. Collectively, the registers contain all the information needed to configure the part, such as data format, mux settings, calibration settings, decimation ratio, etc. Additional registers, such as conversion data, are accessed through dedicated instructions.

The on-chip FLASH can be used to store non-volatile data. The FLASH data is separate from the configuration registers and therefore can be used for any purpose, in addition to device configuration. The FLASH page data is read and written in 128 byte blocks through the RAM banks, i.e. all RAM banks map to a single page of FLASH, as shown in Figure 5.

REGISTER BANK TOPOLOGY

The operation of the device is set up through individual registers. The set of the 16 registers required to configure the device is referred to as a Register Bank, as shown in Figure 5.

RAM

Reads and Writes to Registers and RAM occur on a byte basis. However, copies between registers and RAM occurs on a bank basis. The RAM is independent of the Registers, i.e.: the RAM can be used as general-purpose RAM.

The ADS1218 supports any combination of eight analog inputs. With this flexibility, the device could easily support eight unique configurations—one per input channel. In order to facilitate this type of usage, eight separate register banks are available. Therefore, each configuration could be written once and recalled as needed without having to serially retransmit all the configuration data. Checksum commands are also included, which can be used to verify the integrity of RAM.

The RAM provides eight “banks”, with a bank consisting of 16 bytes. The total size of the RAM is 128 bytes. Copies between the registers and RAM are performed on a bank basis. Also, the RAM can be directly read or written through the serial interface on power-up. The banks allow separate storage of settings for each input.

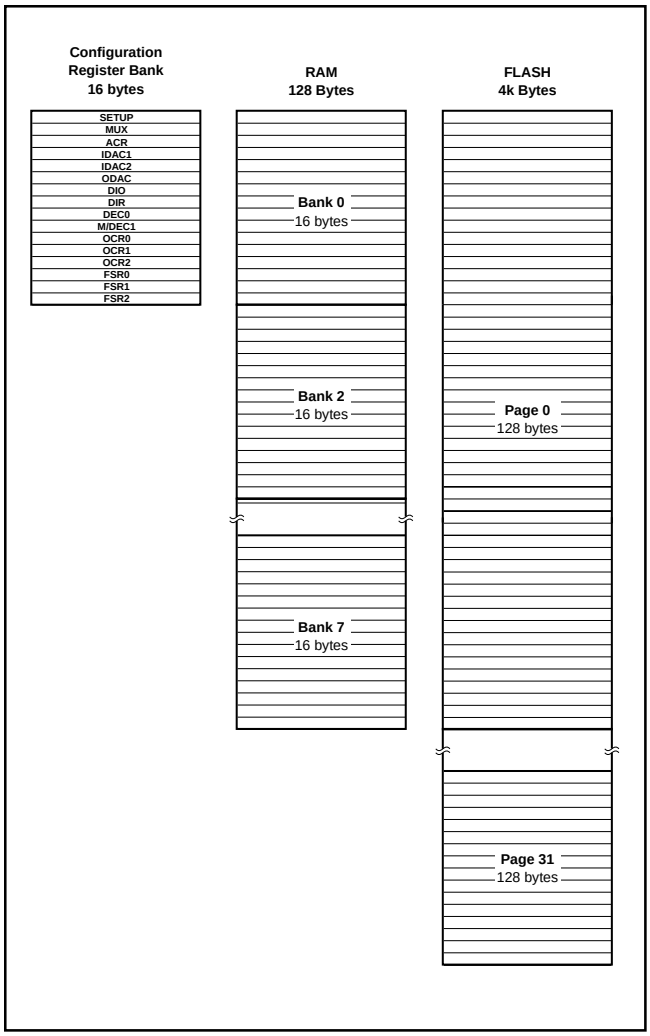


FIGURE 5. Memory Organization.

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00_H	**SETUP**	ID	ID	ID	SPEED	REF EN	REF HI	BUF EN	BIT ORDER
01_H	**MUX**	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02_H	**ACR**	BOCS	IDAC2R1	IDAC2R0	IDAC1R1	IDAC1R0	PGA2	PGA1	PGA0
03_H	**IDAC1**	IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0
04_H	**IDAC2**	IDAC2_7	IDAC2_6	IDAC2_5	IDAC2_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0
05_H	**ODAC**	SIGN	OSET_6	OSET_5	OSET_4	OSET_3	OSET_2	OSET_1	OSET_0
06_H	**DIO**	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
07_H	**DIR**	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
08_H	**DEC0**	DEC07	DEC06	DEC05	DEC04	DEC03	DEC02	DEC01	DEC00
09_H	**M/DEC1**	$\overline{DRDY}$	U/$\overline{B}$	SMODE1	SMODE0	WREN	DEC10	DEC09	DEC08
$0A_H$	**OCR0**	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
$0B_H$	**OCR1**	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
$0C_H$	**OCR2**	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
$0D_H$	**FSR0**	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
$0E_H$	**FSR1**	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
$0F_H$	**FSR2**	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

TABLE II. Registers.

The RAM address space is linear, therefore accessing RAM is done using an auto-incrementing pointer. Access to RAM in the entire memory map can be done consecutively without having to address each bank individually. For example, if you were currently accessing bank 0 at offset 0xF (the last location of bank 0), the next access would be bank 1 and offset 0x0. Any access after bank 7 and offset 0xF will wrap around to bank 0 and Offset 0x0.

Although the Register Bank memory is linear, the concept of addressing the device can also be thought of in terms of bank and offset addressing. Looking at linear and bank addressing syntax, we have the following comparison: in the linear memory map, the address 0x14 is equivalent to bank 1 and offset 0x4. Simply stated, the most significant four bits represent the bank, and the least significant four bits represent the offset. The offset is equivalent to the register address for that bank of memory.

FLASH

Reads and Writes to FLASH occur on a Page basis. Therefore, the entire contents of RAM is used for both Read and Write operations. The FLASH is independent of the Registers, i.e., the FLASH can be used as general-purpose FLASH.

Upon power-up or reset, the contents of FLASH Page 0 are loaded into RAM subsequently the contents of RAM Bank 0 are loaded into the configuration register. Therefore, the user can customize the power-up configuration for the device. Care should be taken to ensure that data for FLASH Page 0 is written correctly, in order to prevent unexpected operation upon power-up.

The ADS1218 supports any combination of eight analog inputs and the FLASH memory supports up to 32 unique Page configurations. With this flexibility, the device could support 32 unique configurations for each of the eight analog input channels. For instance, the on-chip temperature sensor could be used to monitor temperature then different calibration coefficients could be recalled for each of the eight analog input channels based on the change in temperature. This would enable the user to recall calibration coefficients for every 4°C change in temperature over the industrial temperature range which could be used to correct for drift errors. Checksum commands are also included, which can be used to verify the integrity of FLASH.

The following two commands can be used to manipulate the FLASH. First, the contents of FLASH can be written to with the WR2F (write RAM to FLASH) command. This command first erases the designated FLASH page and then writes the entire content of RAM (all banks) into the designated FLASH page. Second, the contents of FLASH can be read with the RF2R (read FLASH to RAM) command. This command reads the designated FLASH page into the entire contents of RAM (all banks). In order to ensure maximum endurance and data retention, the SPEED bit in the SETUP register must be set for the appropriate f_{OSC} frequency.

Writing to or erasing FLASH can be disabled either through the WREN pin or the WREN register bit. If the WREN pin is LOW OR the WREN bit is cleared, then the WR2F command has no effect. This protects the integrity of the FLASH data from being inadvertently corrupted.

Accessing the FLASH data either through read, write, or erase may effect the accuracy of the conversion result. Therefore, the conversion result should be discarded when accesses to FLASH are done.

DETAILED REGISTER DEFINITIONS

SETUP (Address 00_H) Setup Register
Reset Value = iii01110

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ID	ID	ID	SPEED	REF EN	REF HI	BUF EN	BIT ORDER

bit 7-5 Factory Programmed Bits

bit 4 SPEED: FLASH Access Clock Speed
0 : 2.30MHz > f_{OSC} > 3.12MHz (default)
1 : 3.12MHz > f_{OSC} > 4.13MHz

bit 3 REF EN: Internal Voltage Reference Enable
0 = Internal Voltage Reference Disabled
1 = Internal Voltage Reference Enabled (default)

bit 2 REF HI: Internal Reference Voltage Select
0 = Internal Reference Voltage = 1.25V
1 = Internal Reference Voltage = 2.5V (default)

bit 1 BUF EN: Buffer Enable
0 = Buffer Disabled
1 = Buffer Enabled (default)

bit 0 BIT ORDER: Set Order Bits are Transmitted
0 = Most Significant Bit Transmitted First (default)
1 = Least Significant Bit Transmitted First
Data is always shifted into the part most significant bit first. Data is always shifted out of the part most significant byte first. This configuration bit only controls the bit order within the byte of data that is shifted out.

MUX (Address 01_H) Multiplexer Control Register
Reset Value = 01_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select
0000 = AIN0 (default)
0001 = AIN1
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
1xxx = AINCOM (except when all bits are 1's)
1111 = Temperature Sensor Diode Anode

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select
0000 = AIN0
0001 = AIN1 (default)
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
1xxx = AINCOM (except when all bits are 1's)
1111 = Temperature Sensor Diode Cathode Analog GND

ACR (Address 02_H) Analog Control Register
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BOCS	IDAC2R1	IDAC2R0	IDAC1R1	IDAC1R0	PGA2	PGA1	PGA0

bit 7 BOCS: Burnout Current Source
0 = Disabled (default)
1 = Enabled

$$\text{IDAC Current} = \left(\frac{V_{REF}}{8 \bullet R_{DAC}}\right)\left(2^{\text{RANGE}-1}\right)(\text{DAC Code})$$

bit 6-5 IDAC2R1: IDAC2R0: Full-Scale Range Select for IDAC2
00 = Off (default)
01 = Range 1
10 = Range 2
11 = Range 3

bit 4-3 IDAC1R1: IDAC1R0: Full-Scale Range Select for IDAC1
00 = Off (default)
01 = Range 1
10 = Range 2
11 = Range 3

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier
Gain Selection
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

IDAC1 (Address 03_H) Current DAC 1
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0

The DAC code bits set the output of DAC1 from 0 to full-scale. The value of the full-scale current is set by this Byte, V_{REF}, R_{DAC}, and the DAC1 range bits in the ACR register.

IDAC2 (Address 04_H) Current DAC 2
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IDAC2_7	IDAC2_6	IDAC2_5	IDAC2_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0

The DAC code bits set the output of DAC2 from 0 to full-scale. The value of the full-scale current is set by this Byte, V_{REF}, R_{DAC}, and the DAC2 range bits in the ACR register.

ODAC (Address 05_H) Offset DAC Setting
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

bit 7 Offset Sign
0 = Positive
1 = Negative

bit 6-0 $\text{Offset} = \frac{V_{REF}}{2 \bullet PGA} \bullet \left(\frac{\text{Code}}{127}\right)$

NOTE: Calibration will cancel the value in the ODAC register. Therefore, writing to the ODAC register should be done after calibration.

DIO (Address 06_H) Digital I/O Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

A value written to this register will appear on the digital I/O pins if the pin is configured as an output in the DIR register. Reading this register will return the value of the digital I/O pins.

DIR (Address 07_H) Direction control for digital I/O
Reset Value = FF_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Each bit controls whether the Digital I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

DEC0 (Address 08_H) Decimation Register
(Least Significant 8 bits)

Reset Value = 80_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DEC07	DEC06	DEC05	DEC04	DEC03	DEC02	DEC01	DEC00

The decimation value is defined with 11 bits for a range of 20 to 2047. This register is the least significant 8 bits. The 3 most significant bits are contained in the M/DEC1 register. The default data rate is 10Hz with a 2.4576MHz crystal.

M/DEC1 (Address 09_H) Mode and Decimation Register
Reset Value = 07_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SMODE1	SMODE0	WREN	DEC10	DEC09	DEC08

bit 7 $\overline{\text{DRDY}}$: Data Ready (Read Only)
This bit duplicates the state of the $\overline{\text{DRDY}}$ pin.

bit 6 U/$\overline{\text{B}}$: Data Format
0 = Bipolar (default)
1 = Unipolar

U/$\overline{\text{B}}$	ANALOG INPUT	DIGITAL OUTPUT
0	+FSR	0x7FFFFF
	Zero	0x000000
	–FSR	0x800000
1	+FSR	0xFFFFFF
	Zero	0x000000
	–FSR	0x000000

bit 5-4 SMODE1: SMODE0: Settling Mode
00 = Auto (default)
01 = Fast Settling filter
10 = $Sinc^2$ filter
11 = $Sinc^3$ Flash filter

bit 3 WREN: Write Enable
0 = Flash Writing Disabled (default)
1 = Flash Writing Enabled
This bit is AND'd with the WREN pin to enable or disable Flash Writing and Erasing

bit 2-0 DEC10: DEC09: DEC08: Most Significant Bits of the Decimation Value

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OCR0 (Address $0A_H$) Offset Calibration Coefficient
(Least Significant Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 (Address $0B_H$) Offset Calibration Coefficient
(Middle Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 (Address $0C_H$) Offset Calibration Coefficient
(Most Significant Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 (Address $0D_H$) Full-Scale Register
(Least Significant Byte)
Reset Value = 24_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 (Address $0E_H$) Full-Scale Register
(Middle Byte)
Reset Value = 90_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR15	FSR14	FSR13	FSR12	FSR011	FSR10	FSR09	FSR08

FSR2 (Address $0F_H$) Full-Scale Register
(Most Significant Byte)
Reset Value = 67_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR23	FSR22	FSR21	FSR20	FSR019	FSR18	FSR17	FSR16

COMMAND DEFINITIONS

The commands listed below control the operation of the ADS1218. Some of the commands are stand-alone commands (e.g., RESET) while others require additional bytes (e.g., WREG requires command, count, and the data bytes). Commands that output data require a minimum of four f_{OSC} cycles before the data is ready (e.g., RDATA).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

a = RAM bank address (0 to 7)

f = FLASH page address (0 to 31)

COMMANDS	DESCRIPTION	COMMAND BYTE	2ND COMMAND BYTE
RDATA	Read Data	0000 0001 (01_H)	—
RDATAC	Read Data Continuously	0000 0011 (03_H)	—
STOPC	Stop Read Data Continuously	0000 1111 ($0F_H$)	—
RREG	Read from REG Bank "rrrr"	0001 rrrr ($1x_H$)	xxxx_nnnn (# of reg-1)
RRAM	Read from RAM Bank "aaa"	0010 0aaa ($2x_H$)	xnnn_nnnn (# of bytes-1)
CREG	Copy REGs to RAM Bank "aaa"	0100 0aaa ($4x_H$)	—
CREGA	Copy REGS to all RAM Banks	0100 1000 (48_H)	—
WREG	Write to REG "rrrr"	0101 rrrr ($5x_H$)	xxxx_nnnn (# of reg-1)
WRAM	Write to RAM Bank "aaa"	0110 0aaa ($6x_H$)	xnnn_nnnn (# of bytes-1)
RF2R	Read FLASH page to RAM	100f ffff ($8,9x_H$)	—
WR2F	Write RAM to FLASH page	101f ffff (A,Bx_H)	—
CRAM	Copy RAM Bank "aaa" to REG	1100 0aaa (Cx_H)	—
CSRAMX	Calc RAM Bank "aaa" Checksum	1101 0aaa (Dx_H)	—
CSARAMX	Calc all RAM Bank Checksum	1101 1000 ($D8_H$)	—
CSREG	Calc REG Checksum	1101 1111 (DF_H)	—
CSRAM	Calc RAM Bank "aaa" Checksum	1110 0aaa (Ex_H)	—
CSARAM	Calc all RAM Banks Checksum	1110 1000 ($E8_H$)	—
CSFL	Calc FLASH Checksum	1110 1100 (EC_H)	—
SELFCAL	Self Cal Offset and Gain	1111 0000 ($F0_H$)	—
SELFOCAL	Self Cal Offset	1111 0001 ($F1_H$)	—
SELFGCAL	Self Cal Gain	1111 0010 ($F2_H$)	—
SYSOCAL	Sys Cal Offset	1111 0011 ($F3_H$)	—
SYSGCAL	Sys Cal Gain	1111 0100 ($F4_H$)	—
DSYNC	Sync $\overline{DRDY}$	1111 1100 (FC_H)	—
SLEEP	Put in SLEEP Mode	1111 1101 (FD_H)	—
RESET	Reset to Power-Up Values	1111 1110 (FE_H)	—

NOTE: (1) The data received by the A/D is always MSB First, the data out format is set by the BIT ORDER bit in ACR reg.

TABLE III. Command Summary.

RDATA Read Data

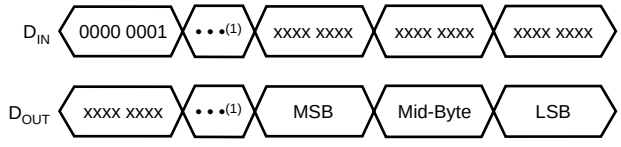
Description: Read a single data value from the Data Output Register (DOR) which is the most recent conversion result. This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE: (1) For wait time, refer to timing specification.

RDATAC Read Data Continuous

Description: Read Data Continuous mode enables the continuous output of new data on each $\overline{DRDY}$. This command eliminates the need to send the Read Data Command on each $\overline{DRDY}$. This mode may be terminated by either the STOP Read Continuous command or the RESET command.

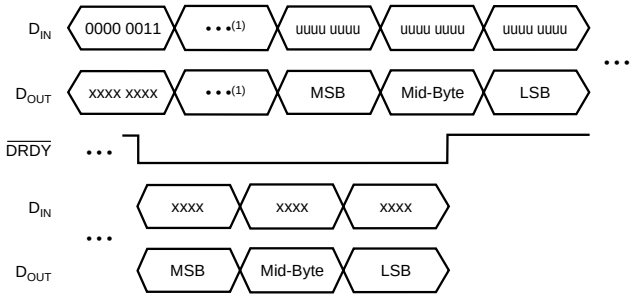
Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:

Command terminated when "uuuu uuuu" equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

STOPC Stop Continuous

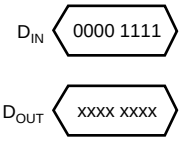
Description: Ends the continuous data output mode.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

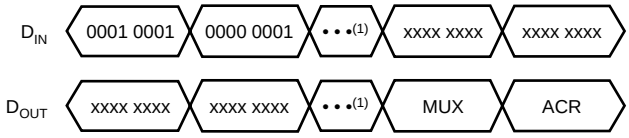
Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:

Read Two Registers Starting from Register 01_H (MUX)



NOTE: (1) For wait time, refer to timing specification.

RRAM Read from RAM

Description: Up to 128 bytes can be read from RAM starting at the bank specified in the op code. All reads start at the address for the beginning of the RAM bank. The number of bytes to read will be one plus the value of the second byte.

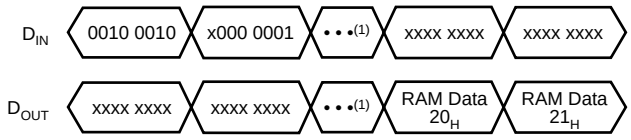
Operands: a, n

Bytes: 2

Encoding: 0010 0aaa xnnn nnnn

Data Transfer Sequence:

Read Two RAM Locations Starting from 20_H



NOTE: (1) For wait time, refer to timing specification.

CREG Copy Registers to RAM Bank

Description: Copy the 16 control registers to the RAM bank specified in the op code. Refer to timing specifications for command execution time.

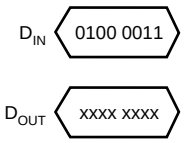
Operands: a

Bytes: 1

Encoding: 0100 0aaa

Data Transfer Sequence:

Copy Register Values to RAM Bank 3



CREGA Copy Registers to All RAM Banks

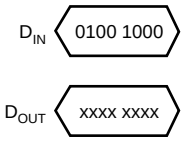
Description: Duplicate the 16 control registers to all the RAM banks. Refer to timing specifications for command execution time.

Operands: None

Bytes: 1

Encoding: 0100 1000

Data Transfer Sequence:



WREG Write to Register

Description: Write to the registers starting with the register specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

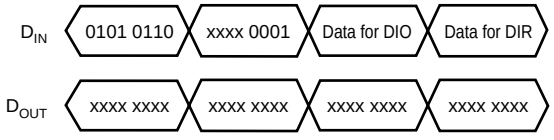
Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:

Write Two Registers Starting from 06_H (DIO)



WRAM Write to RAM

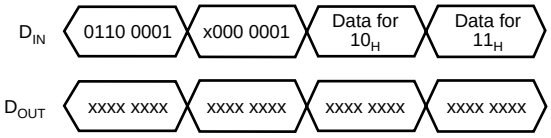
Description: Write up to 128 RAM locations starting at the beginning of the RAM bank specified as part of the instruction. The number of bytes written is RAM is one plus the value of the second byte.

Operands: a, n

Bytes: 2

Encoding: 0110 0aaa xnnn nnnn

Data Transfer Sequence:
Write to Two RAM Locations starting from 10_H



RF2R Read FLASH Page to RAM

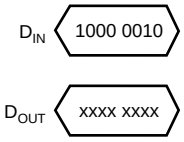
Description: Read the selected FLASH page to the RAM.

Operands: f

Bytes: 1

Encoding: 100f ffff

Data Transfer Sequence:
Read FLASH Page 2 to RAM



WR2F Write RAM to FLASH

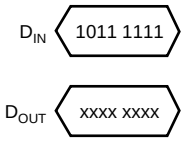
Description: Write the contents of RAM to the selected FLASH page.

Operands: f

Bytes: 1

Encoding: 101f ffff

Data Transfer Sequence:
Write RAM to FLASH page 31



CRAM Copy RAM Bank to Registers

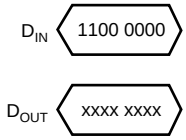
Description: Copy the selected RAM Bank to the Configuration Registers. This will overwrite all of the registers with the data from the RAM bank.

Operands: a

Bytes: 1

Encoding: 1100 0aaa

Data Transfer Sequence:
Copy RAM Bank 0 to the Registers



CSRAMX Calculate RAM Bank Checksum

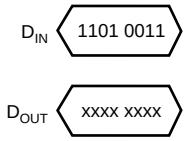
Description: Calculate the checksum of the selected RAM Bank. The checksum is calculated as a sum of all the bytes with the carry ignored. The ID, $\overline{DRDY}$ and DIO bits are masked so they are not included in the checksum.

Operands: a

Bytes: 1

Encoding: 1101 0aaa

Data Transfer Sequence:
Calculate Checksum for RAM Bank 3



CSARAMX Calculate the Checksum for all RAM Banks

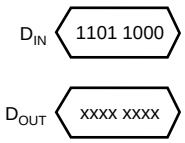
Description: Calculate the checksum of all RAM Banks. The checksum is calculated as a sum of all the bytes with the carry ignored. The ID, $\overline{DRDY}$ and DIO bits are masked so they are not included in the checksum.

Operands: None

Bytes: 1

Encoding: 1101 1000

Data Transfer Sequence:



CSREG Calculate the Checksum of Registers

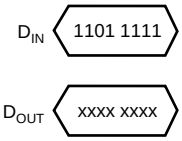
Description: Calculate the checksum of all the registers. The checksum is calculated as a sum of all the bytes with the carry ignored. The ID, $\overline{\text{DRDY}}$ and DIO bits are masked so they are not included in the checksum.

Operands: None

Bytes: 1

Encoding: 1101 1111

Data Transfer Sequence:



CSRAM Calculate RAM Bank Checksum

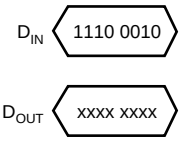
Description: Calculate the checksum of the selected RAM Bank. The checksum is calculated as a sum of all the bytes with the carry ignored. All bits are included in the checksum calculation, there is no masking of bits.

Operands: a

Bytes: 1

Encoding: 1110 0aaa

Data Transfer Sequence:
Calculate Checksum for RAM Bank 2



CSARAM Calculate Checksum for all RAM Banks

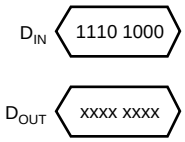
Description: Calculate the checksum of all RAM Banks. The checksum is calculated as a sum of all the bytes with the carry ignored. All bits are included in the checksum calculation, there is no masking of bits.

Operands: None

Bytes: 1

Encoding: 1110 1000

Data Transfer Sequence:



CSFL Calculate Checksum for all FLASH Pages

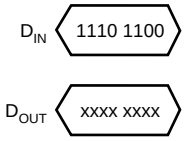
Description: Calculate the checksum for all FLASH pages. The checksum is calculated as a sum of all the bytes with the carry ignored. All bits are included in the checksum calculation, there is no masking of bits.

Operands: None

Bytes: 1

Encoding: 1110 1100

Data Transfer Sequence:



SELFCAL Offset and Gain Self Calibration

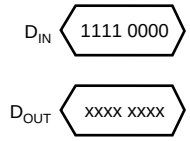
Description: Starts the process of self calibration. The Offset Control Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL Offset Self Calibration

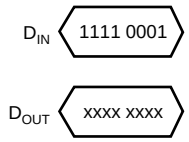
Description: Starts the process of self-calibration for offset. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL Gain Self Calibration

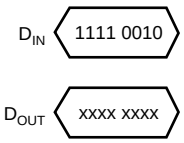
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL System Offset Calibration

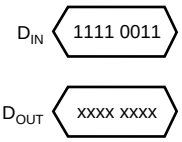
Description: Starts the system offset calibration process. For a system offset calibration the input should be set to 0V differential, and the ADS1218 computes the OCR register value that will compensate for offset errors. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL System Gain Calibration

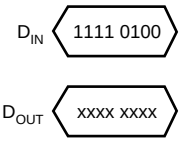
Description: Starts the system gain calibration process. For a system gain calibration, the differential input should be set to the reference voltage and the ADS1218 computes the FSR register value that will compensate for gain errors. The FSR is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0100

Data Transfer Sequence:



DSYNC Sync $\overline{\text{DRDY}}$

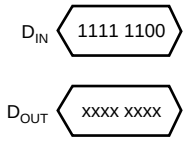
Description: Synchronizes the ADS1218 to the serial clock edge.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence:



SLEEP Sleep Mode

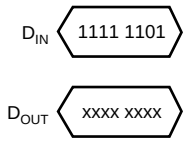
Description: Puts the ADS1218 into a low power sleep mode. To exit sleep mode strobe SCLK.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence:



RESET Reset to Powerup Values

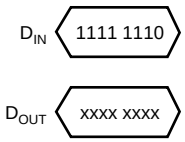
Description: Restore the registers to their power-up values. This command will also stop the Read Continuous mode. It does not affect the contents of RAM.

Operands: None

Bytes: 1

Encoding: 1111 1110

Data Transfer Sequence:



MSB	LSB 0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	x	rdata	x	rdatac	x	x	x	x	x	x	x	x	x	x	x	stopc
0001	rreg 0	rreg 1	rreg 2	rreg 3	rreg 4	rreg 5	rreg 6	rreg 7	rreg 8	rreg 9	rreg A	rreg B	rreg C	rreg D	rreg E	rreg F
0010	rram 0	rram 1	rram 2	rram 3	rram 4	rram 5	rram 6	rram 7	x	x	x	x	x	x	x	x
0011	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0100	creg 0	creg 1	creg 2	creg 3	creg 4	creg 5	creg 6	creg 7	crega	x	x	x	x	x	x	x
0101	wreg 0	wreg 1	wreg 2	wreg 3	wreg 4	wreg 5	wreg 6	wreg 7	wreg 8	wreg 9	wreg A	wreg B	wreg C	wreg D	wreg E	wreg F
0110	wram 0	wram 1	wram 2	wram 3	wram 4	wram 5	wram 6	wram 7	x	x	x	x	x	x	x	x
0111	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1000	rf2r 0	rf2r 1	rf2r 2	rf2r 3	rf2r 4	rf2r 5	rf2r 6	rf2r 7	rf2r 8	rf2r 9	rf2r A	rf2r B	rf2r C	rf2r D	rf2r E	rf2r F
1001	rf2r 10	rf2r 11	rf2r 12	rf2r 13	rf2r 14	rf2r 15	rf2r 16	rf2r 17	rf2r 18	rf2r 19	rf2r 1A	rf2r 1B	rf2r 1C	rf2r 1D	rf2r 1E	rf2r 1F
1010	wr2f 0	wr2f 1	wr2f 2	wr2f 3	wr2f 4	wr2f 5	wr2f 6	wr2f 7	wr2f 8	wr2f 9	wr2f A	wr2f B	wr2f C	wr2f D	wr2f E	wr2f F
1011	wr2f 10	wr2f 11	wr2f 12	wr2f 13	wr2f 14	wr2f 15	wr2f 16	wr2f 17	wr2f 18	wr2f 19	wr2f 1A	wr2f 1B	wr2f 1C	wr2f 1D	wr2f 1E	wr2f 1F
1100	cram 0	cram 1	cram 2	cram 3	cram 4	cram 5	cram 6	cram 7	x	x	x	x	x	x	x	x
1101	csramx 0	csramx 1	csramx 2	csramx 3	csramx 4	csramx 5	csramx 6	csramx 7	csramx	x	x	x	x	x	x	csreg
1110	csram 0	csram 1	csram2	csram 3	csram 4	csram 5	csram 6	csram 7	csram	x	x	x	csfl	x	x	x
1111	self cal	self ocal	self gcal	sys ocal	sys gcal	x	x	x	x	x	x	x	dsync	sleep	reset	x

x = Reserved

TABLE IV. ADS1218 Command Map.

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI), allows a controller to communicate synchronously with the ADS1218. The ADS1218 operates in slave only mode.

SPI Transfer Formats

During an SPI transfer, data is simultaneously transmitted and received. The SCLK signal synchronizes shifting and sampling of the information on the two serial data lines: D_{IN} and D_{OUT}. The $\overline{CS}$ signal allows individual selection of an ADS1218 device; an ADS1218 with $\overline{CS}$ HIGH is not active on the bus.

Clock Phase and Polarity Controls (POL)

The clock polarity is specified by the POL pin, which selects an active HIGH or active LOW clock, and has no effect on the transfer format.

Serial Clock (SCLK)

SCLK, a Schmitt Trigger input to the ADS1218, is generated by the master device and synchronizes data transfer on the D_{IN} and D_{OUT} lines. When transferring data to or from the ADS1218, burst mode may be used i.e., multiple bits of data may be transferred back-to-back with no delay in SCLKs or toggling of $\overline{CS}$.

Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input of the ADS1218 must be externally asserted before a master device can exchange data with the ADS1218. $\overline{CS}$ must be LOW before data transactions and must stay LOW for the duration of the transaction.

DIGITAL INTERFACE

The ADS1218's programmable functions are controlled using a set of on-chip registers, as outlined previously. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface.

The ADS1218's serial interface consists of four signals: $\overline{CS}$, SCLK, D_{IN}, and D_{OUT}. The D_{IN} line is used for transferring data into the on-chip registers while the D_{OUT} line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on D_{IN} or D_{OUT}) take place with respect to this SCLK signal.

The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the ADS1218's data register. $\overline{DRDY}$ goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

$\overline{CS}$ is used to select the device. It can be used to decode the ADS1218 in systems where a number of parts are connected to the serial bus.

The timing specification shows the timing diagram for interfacing to the ADS1218 with $\overline{CS}$ used to decode the part.

The ADS1218 serial interface can operate in three-wire mode by tying the $\overline{CS}$ input LOW. In this case, the SCLK, D_{IN}, and D_{OUT} lines are used to communicate with the ADS1218 and the status of $\overline{DRDY}$ can be obtained by interrogating bit 7 of the M/DEC1 register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin.

DEFINITION OF TERMS

Analog Input Voltage—the voltage at any one analog input relative to AGND.

Analog Input Differential Voltage—given by the following equation: (IN+ – IN–). Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the AGND to AV_{DD} range.

Conversion Cycle—the term "conversion cycle" usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period. However, each digital output is actually based on the modulator results from several t_{DATA} time periods.

FILTER SETTING	MODULATOR RESULTS
fast settling	1 t_{DATA} time period
$sinc^2$	2 t_{DATA} time period
$sinc^3$	3 t_{DATA} time period

Data Rate—The rate at which conversions are completed. See definition for f_{DATA}.

Decimation Ratio—defines the ratio between the output of the modulator and the output Data Rate. Valid values for the Decimation Ratio are from 20 to 2047. Larger Decimation Ratios will have lower noise and vice-versa.

Effective Resolution—the effective resolution of the ADS1218 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and Vrms (referenced to input). Computed directly from the converter's output data, each is a statistical calculation. The conversion from one to the other is shown below.

BITS rms	BIPOLAR Vrms	UNIPOLAR Vrms
	$\frac{\left(\frac{2 \bullet V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \bullet ER}{20}\right)}}$	$\frac{\left(\frac{V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \bullet ER}{20}\right)}}$
24	298nV	149nV
22	1.19µV	597nV
20	4.77µV	2.39µV
18	19.1µV	9.55µV
16	76.4µV	38.2µV
14	505µV	152.7µV
12	1.22mV	610µV

Filter Selection—the ADS1218 uses a (sinx /x) filter or sinc filter. Actually there are three different sinc filters that can be selected. A fast settling filter will settle in one t_{DATA} cycle. The $sinc^2$ filter will settle in two cycles and have lower noise. The $sinc^3$ will achieve the lowest noise and highest number of effective bits, but requires three cycles to settle. The ADS1218 will operate with any one of these filters, or it can operate in an auto mode, where it will select the fast settling filter after a new channel is selected and will then switch to $sinc^2$ followed by $sinc^3$. This allows fast settling response and still achieves low noise after the necessary number of t_{DATA} cycles.

f_{OSC}—the frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1218.

f_{MOD}—the frequency or speed at which the modulator of the ADS1218 is running. This depends on the SPEED bit as given by the following equation:

	SPEED = 0	SPEED = 1
mfactor	128	256

$$f_{MOD} = \frac{f_{OSC}}{mfactor}$$

f_{SAMP}—the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

PGA SETTING	SAMPLING FREQUENCY
1, 2, 4, 8	$f_{SAMP} = \frac{f_{OSC}}{mfactor}$
16	$f_{SAMP} = \frac{f_{OSC} \bullet 2}{mfactor}$
32	$f_{SAMP} = \frac{f_{OSC} \bullet 4}{mfactor}$
64, 128	$f_{SAMP} = \frac{f_{OSC} \bullet 8}{mfactor}$

f_{DATA}—the frequency of the digital output data produced by the ADS1218, f_{DATA} is also referred to as the Data Rate.

$$f_{DATA} = \left(\frac{f_{MOD}}{\text{Decimation Ratio}}\right) = \left(\frac{f_{OSC}}{\text{mfactor} \bullet \text{Decimation Ratio}}\right)$$

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1218 is defined as the "input", which produces the positive full-scale digital output minus the "input", which produces the negative full-scale digital output. The full-scale range changes with gain setting as shown in Table V.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) minus –1.25V (negative full-scale)] = 2.5V.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full-Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

t_{DATA}—the inverse of f_{DATA}, or the period between each data output.

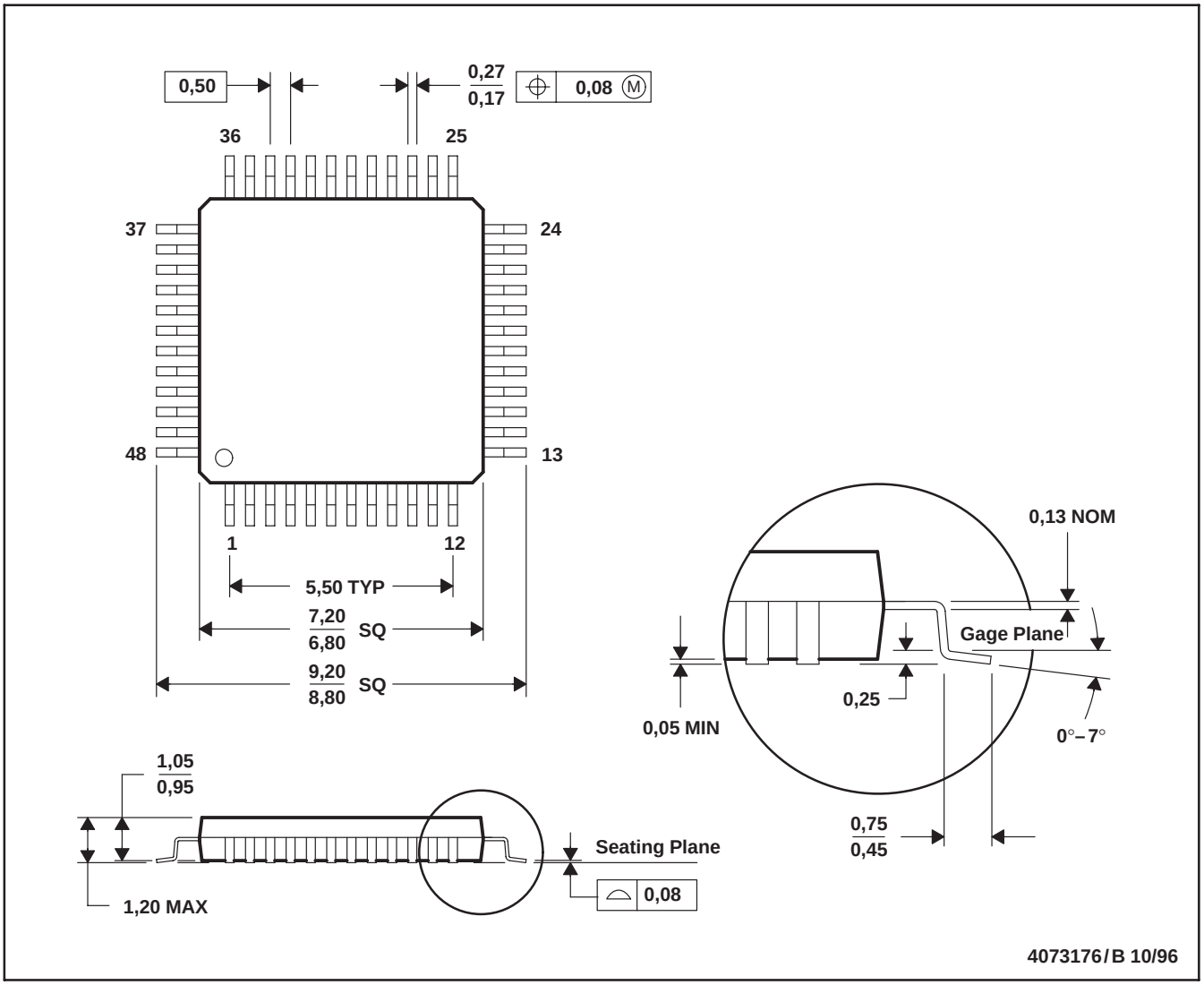
	5V SUPPLY ANALOG INPUT(1)			GENERAL EQUATIONS		
GAIN SETTING	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA OFFSET RANGE	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA SHIFT RANGE
1	5V	±2.5V	±1.25V	$\frac{2 \bullet V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{2 \bullet PGA}$
2	2.5V	±1.25V	±0.625V			
4	1.25V	±0.625V	±312.5mV			
8	0.625V	±312.5mV	±156.25mV			
16	312.5mV	±156.25mV	±78.125mV			
32	156.25mV	±78.125mV	±39.0625mV			
64	78.125mV	±39.0625mV	±19.531mV			
128	39.0625mV	±19.531mV	±9.766mV			

NOTES: (1) With a 2.5V reference. (2) The ADS1218 allows common-mode voltage as long as the absolute input voltage on $A_{IN}P$ or $A_{IN}N$ does not go below AGND or above AV_{DD}.

TABLE V. Full-Scale Range versus PGA Setting.

TOPIC INDEX

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
ADS1218Y/250	ACTIVE	TQFP	PFB	48	250
ADS1218Y/2K	ACTIVE	TQFP	PFB	48	2000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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